IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

a dielectric layer on a semiconductor substrate, the dielectric layer comprising a lower diclectric layer and an upper diclectric layer ;

a contact window passing through the dielectric layer;

an upper region of the contact window having a sidewall substantially perpendicular to the substrate; ~~and~~

a lower region of the contact window having a width that increases in a direction toward the substrate; and

a plurality of conductive patterns disposed between the lower diclectric layer and the upper dielectric layer, wherein the conductive patterns are spaced apart from the contact window, wherein one of the plurality of conductive patterns is spaced apart from another one of the plurality of conductive patterns by a sclected distance, and a bottommost width of the contact window is wider than the sclected distance.

2. (Cancelcd)

3. (Canceled)

4. (Currently amended) A semiconductor device comprising:

a dielectric layer on a semiconductor substrate;

a contact window passing through the dielectric layer;

an upper region of the contact window having a sidewall substantially perpendicular to the substrate;

a lower region of the contact window having a wider width than that of the upper region of the contact window; ~~and~~

a spacer on the sidewall; and

a plurality of conductive patterns in the dielectric layer, wherein the plurality of conductive patterns is spaced apart from the contact window.

5. (Canceled)

6. (Currently amended) The semiconductor device of claim 4 ~~claim 5~~, wherein one of the plurality of conductive patterns is spaced apart from another one of the plurality of

conductive patterns with a selected distance, and a bottommost width of the contact window is wider than the selected distance.

7. (Original) The semiconductor device of claim 4 further comprises a capping layer on the dielectric layer.

8. (Original) The semiconductor device of claim 4, wherein the spacer is made of a material selected from the group consisting of polycrystalline silicon, silicon nitride and silicon oxynitride.

9. (Original) The semiconductor device of claim 7, wherein the capping layer is made from a material selected of the group consisting of polycrystalline silicon, silicon nitride and silicon oxynitride.

10. (Currently amended) A semiconductor device comprising:

an interlayer dielectric layer on a semiconductor substrate, wherein the interlayer dielectric layer comprises a first dielectric layer, a second dielectric layer and ~~a~~ an upper dielectric layer;

a contact window passing through the interlayer dielectric layer, wherein a lower region of the contact window has a wider width than that of an upper region of the contact window; and

a plurality of conductive patterns intervening between the second dielectric layer and the upper dielectric layer, wherein the conductive patterns are spaced apart from the contact window, wherein one of the plurality of conductive patterns is spaced apart from another one of the plurality of conductive patterns with a selected distance, and a bottommost width of the contact window is wider than the distance.

11. (Canceled)

12. (Original) The semiconductor device of claim 10, wherein a width of the contact window in the upper dielectric layer is substantially the same as a width of the contact window in the second dielectric layer.